GaAs SEMI-INSULATED-GATE FETs (SIGFETs) AS HIGH POWER MMIC CONTROL DEVICES

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ABSTRACT

GaAs planar Semi-Insulated-Gate FETs (SIGFETs) have been fabricated with higher CW power handling capability than, and similar switching frequency figure-of-merit as, comparable GaAs recess-gate MESFETs. Initially developed SIGFET devices demonstrated 3dB to 5dB increase in power handling capability with a switching frequency figure-of-merit of 362GHz. This improved power performance is due chiefly to the semi-insulated layer under the gate metal, which allows higher gate-breakdown voltage as well as higher drain saturation current.

INTRODUCTION

GaAs MESFETs are recognized as viable RF control devices for applications such as switching and phase shifting, particularly in MMIC implementations. Passive GaAs MESFET two-state control devices have low bias power consumption and fast switching times. Moreover, multioctave bandwidth capability can be achieved since the DC bias terminal (gate) and the RF terminals (source and drain) are easily isolated resistively. The inherent disadvantages of GaAs MESFETs in passive control applications compared to conventional silicon p-i-n diodes are twofold: 1)lower switching frequency figure-of-merit and 2)lower power handling capability. This paper presents initial experimental results to increase the power handling of GaAs MMIC FET control components, while maintaining (and perhaps improving) the switching frequency figure-of-merit using a planar semi-insulated-gate FET (SIGFET) structure(1,2). The GaAs SIGFET's device structure, fabrication, initial experimental results, and comparative advantages to conventional recess-gate GaAs MESFET devices will be discussed in this paper.

SIGFET DEVICE STRUCTURE AND FABRICATION

A photograph of the SIGFET fabricated in this work is shown in Fig.1a with a cross section view depicted in Fig.1b. The gate length is 1 micron, total gate width 260 microns, and spacing between source and drain contacts 3 microns. The fabrication procedure is similar to that for conventional GaAs MESFETs except for creation of the semi-insulated region under the gate metal. The active layer is formed by ion implantation of 200 KeV Si ions with a 8E12 per cm-square dose into a semi-insulating GaAs substrate which is subsequently annealed. The resulting n-layer peak doping concentration is 2.8E17 per cm-cubed at a depth of 0.18 microns, with the doping concentration decreasing to 1.0E17 per cm-cubed at a depth of 0.26 microns. These measured values are compatible with LSS theory. After ohmic-metal formation and planar device isolation, the shallow semi-insulated region with nominal thickness of 0.1 microns is formed between source and drain by ion implantation with low energy boron. This step replaces the gate-recess etch process of conventional GaAs MESFETs and keeps the wafer planar throughout the fabrication process, which is favorable for high yield MMIC manufacturing. One micron gates are then fabricated with Ti/Pt/Au metalization.

DC AND RF EXPERIMENTAL RESULTS

Typical DC characteristics (Fig.2) show a saturated drain current (Idss) = 346mA/mm, pinch-off voltage (Vp) = 10V, and breakdown voltage (Vbr)=22V. Due to the semi-insulated layer under the gate metal, these values are higher than those typically achieved with conventional recess-gate GaAs MESFET control devices(3,4), and result in improved power handling capability. The power handling capability of the devices was tested at 5GHz in a SPST

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series switch configuration at increasing CW power levels in both conducting and non-conducting states. The test results (Fig.3) indicate that a SIGFET can handle 3dB to 5dB more power than that of comparable GaAs MESFETs which were reported earlier(4).

In comparing the switching capabilities of alternative two-states (on and off) devices, the switching frequency figure-of-merit (Fs) approximated by Gutmann et al (3,4) is used in this work, namely

$$Fs = 1 / (2 \pi RC)$$

where R is the conducting (on) state resistance and C is the non-conducting (off) state capacitance between source and drain. The values of R and C of the SIGFETs were obtained from insertion loss and isolation measurements from 50MHz to 18GHz with resulting values of 3.1ohm-mm and 0.14pf/mm, respectively. The switching frequency figure-of-merit (Fs) obtained is 362 GHz. Table-1 shows that the SIGFET parameters are comparable with those of the conventional recess-gate GaAs MESFETs (3,4).

GaAs SIGFET PERFORMANCE COMPARED TO MESFET

The DC characteristics of the SIGFET shown in FIG.2 indicate reasonable FET characteristics, namely non-looping I-V and clean gate breakdown. Moreover, the gate breakdown voltage is approximately compatible with the channel and semi-insulated region parameters presented earlier, while the low transconductance (40 mS/mm) is a result of the voltage drop across the semi-insulated layer. These characteristics, and the increased forward bias turn-on voltage compared to a Schottky gate, are compatible with previous results using proton and argon implantation to form the semi-insulated region (1,2).

The increased power handling of SIGFET in the non-conducting state is attributed to the increased breakdown voltage of the device, as the expected power handling capability is proportional to $(Vbr-Vp)^2$ to first order. The actual devices indicate a further improvement, which is attributed to the large DC biasing employed (close to breakdown as suggested previously in (4)). The increased power handling of the SIGFET in the conducting state is directly dependent upon the increased channel thickness capability for a given nominal doping in the channel and the increased forward bias turn-on voltage for the semi-insulated gate. While the exact improvement depends upon the ion-implantation profiles in the SIGFET compared to the MESFET, the reduction in the channel doping peak near the semi-insulated region is critically important. Moreover, in both states the dynamic response of the semi-insulated gate to larger amplitude RF signals must be considered.

In considering the SIGFET structure in Fig.1b, a high conducting-state resistance could be anticipated from the reduced channel thickness between source and gate as well as between drain and gate. It has been shown that this resistance component is typically half of the total conducting-state resistance for conventional recessed-gate MESFETs(5). However, the thicker channel possible with the SIGFET device, combined with a negligible surface depletion more than compensates the effect of the channel thickness reduction by the boron implant. As indicated in Table-1, the conducting-state resistance and switching figure-of-merit of these initial SIGFETs are comparable to the more developed recessed-gate MESFETs.

CONCLUSIONS

In summary, GaAs planar SIGFETs have been fabricated which demonstrate a 3dB to 5dB increase in CW power handling capability and comparable switching frequency figure-of-merit relative to conventional recess-gate MESFETs. This improved power performance is due chiefly to the semi-insulated layer under the gate metal which allows higher gate-to-drain breakdown voltage and increased drain saturation current. While additional effort is needed to fully evaluate the SIGFET potential, higher power control circuits appears to be quite feasible. Moreover, we expect that manufacturing reproducibility to be enhanced as a gate recess etch is not needed. However, the stability of the semi-insulated region needs to be further evaluated prior to component implementation.

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TABLE 1

Gate-Length (Lg), Gate-Width (Wg), Normalized Saturated Drain Current (Idss), Conducting-State Resistance (R), Nonconducting-State Capacitance (C), and Switching Frequency Figure-Of-Merit (Fs) for Conventional MESFETs and SIGFET.

Device Type	Lg (μm)	Wg (μm)	Idss (mA/mm)	R (ohm-mm)	C (pF/mm)	Fs (GHz)
A*	0.8	400	250	2.2	.23	320
B*	1.0	1200	190	4.8	.14	
C*	0.3	400	225	3.0	.18	
D*	0.3	400	200	2.4	.15	435
E*	1.0	1200	180	3.1	.27	190
F*	1.0	530	290	3.5	.16	290
G*	0.5	530	170	2.2	.15	470
SIGFET	1.0	260	346	3.1	.14	362

*Conventional Recess-Gate GaAs MESFETs From Reference (4).

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FIGURE 1a

The SIGFET with 1 micron gate-length and 260 micron gate-width.

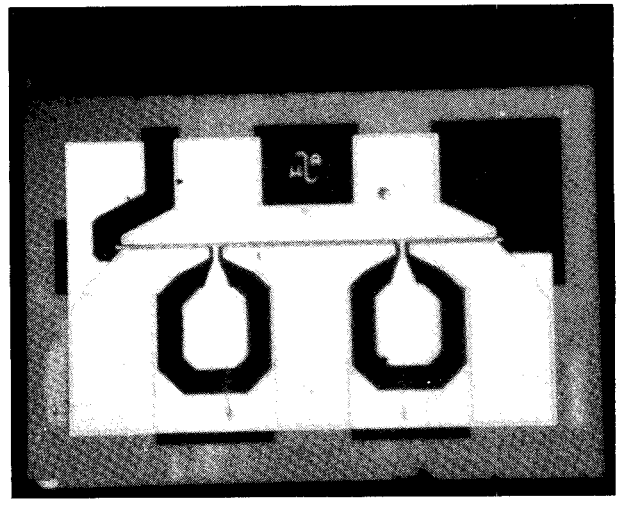
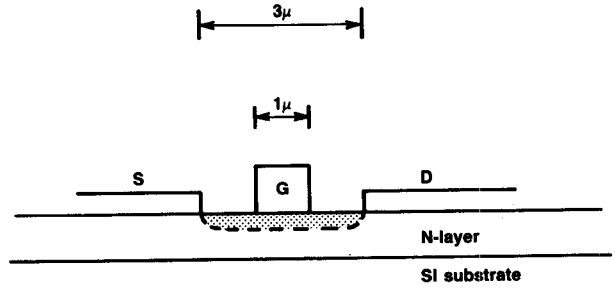


FIGURE 1b



Cross section of the SIGFET.
Dotted area is the semi-insulated layer made by boron ion implantation.

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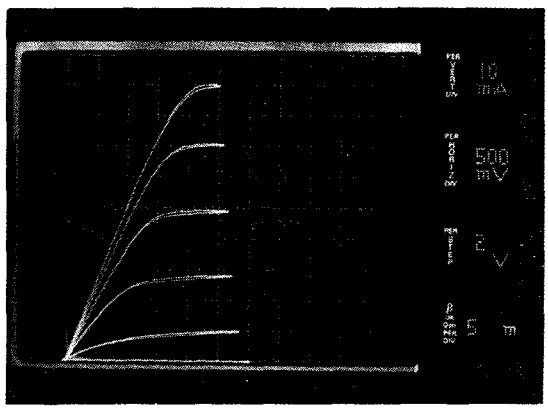
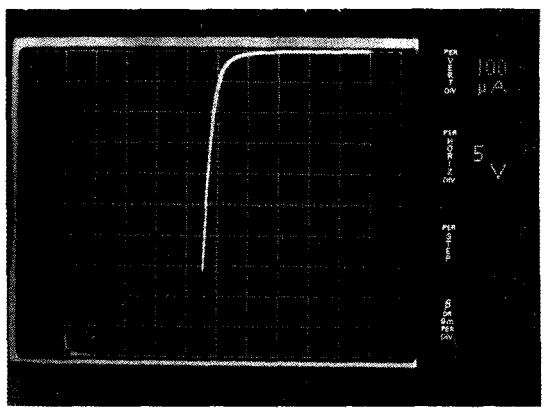
FIGURE 2 : Typical DC characteristics of SIGFETs.

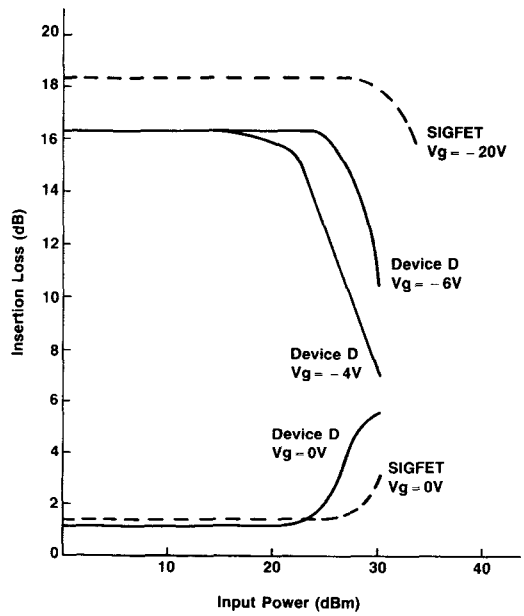


(A) Ids vs. Vds at gate voltages with 2V steps.



(B) Gate reversed breakdown characteristics with common source and drain.

FIGURE 3



Insertion Loss (dB) vs. Input Power (dBm) indicating power handling capabilities of devices in SPST series switch.

Dashed Lines: SIGFET
Solid Lines: Conventional Recess-Gate MESFET Device D From Reference (4).